WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a plurality of first signal lines formed on the insulating substrate;

a plurality of second signal lines formed on the insulating substrate and intersecting the first wire in an insulating manner;

a pixel electrode formed in a pixel area defined by the intersections of the first signal lines and the second signal lines and including a plurality of subareas partitioned by cutouts and a plurality of bridges connecting the subareas; and

a direction control electrode formed in the pixel area and including a portion overlapping at least one of the cutouts,

wherein two long edges of each subarea are parallel to each other and the at least one of cutouts overlapping the portion of the direction control electrode defines one of two longest edges of the subarea.

2. The thin film transistor array panel of claim 1, further comprising a third signal line intersecting the second signal lines in an insulating manner and including a portion overlapping at least another of the cutouts which is not overlapping the direction control electrode.

3. The thin film transistor array panel of claim 2, wherein the third signal line comprises a pair of portions placed between adjacent two of the first signal lines and having inversion symmetry.

4. The thin film transistor array panel of claim 3, wherein the pair of portions of the third signal line placed between the adjacent two of the first signal lines are connected to each other through a connector.

5. The thin film transistor array panel of claim 1, further comprising:

a first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines, and the pixel electrode;

a second thin film transistor connected to a previous one of the first signal lines, a previous one of the second signal lines, and the direction control electrode; and

a third thin film transistor connected to the previous first signal line, the relevant second signal line, and the pixel electrode.

6. The thin film transistor array panel of claim 1, wherein at least one of the bridges are located near a center of the long edges of the subareas and the other of the bridges are located at an edge of the pixel electrode positioned close to the second signal lines.

7. The thin film transistor array panel of claim 1, wherein the bridges are located at an edge of the pixel electrode positioned close to the second signal lines.

8. The thin film transistor array panel of claim 1, wherein at least one of the subareas is chamfered.

9. The thin film transistor array panel of claim 1, wherein the cutouts comprise a transverse cutout bisecting the pixel electrode into upper and lower halves and a plurality of oblique cutouts having inversion symmetry with respect to the transverse cutout.

10. The thin film transistor array panel of claim 9, wherein the oblique cutouts comprise:

a first cutout proceeding from an edge of the pixel electrode toward another edge of the pixel electrode to define one of the bridges located between a terminal of the first cutout and the another edge of the pixel electrode;

a second cutout proceeding from an edge of the pixel electrode into the pixel electrode;

a third cutout proceeding from the transverse cutout into the pixel electrode, the second and the third cutouts running in a straight line to define one of the bridges located between the second cutout and the third cutout; and

a pair of fourth cutouts proceeding from edges of the pixel electrode into the pixel electrode and extending along a straight line to define one of the bridges located between the fourth cutouts.

11. The thin film transistor array panel of claim 9, wherein the oblique cutouts comprise:

a first cutout proceeding from an edge of the pixel electrode toward another edge of the pixel electrode to define one of the bridges located between a terminal of the first cutout and the another edge of the pixel electrode; and

a second cutout curved to define both a long edge and a short edge of one of the subareas.

12. The thin film transistor array panel of claim 9, wherein the oblique cutouts comprise:

a first cutout proceeding from an edge of the pixel electrode toward another edge of the pixel electrode to define one of the bridges located between a terminal of the first cutout and the another edge of the pixel electrode;

a second cutout proceeding from an edge of the pixel electrode toward the transverse cutout to define one of the bridges located between the transverse cutout and a terminal of the second cutout; and

a pair of third cutouts proceeding from edges of the pixel electrode into the pixel electrode and extending along a straight line to define one of the bridges located between the fourth cutouts.

13. The thin film transistor array panel of claim 12, wherein the second and the third cutouts have inlets wider than the terminals of the second and the third cutouts.

14. The thin film transistor array panel of claim 9, wherein the oblique cutouts comprise:

a first cutout proceeding from an edge of the pixel electrode toward another edge of the pixel electrode to define one of the bridges located between a terminal of the first cutout and the another edge of the pixel electrode;

a second cutout proceeding from an edge of the pixel electrode toward the transverse cutout to define one of the bridges located between the transverse cutout and a terminal of the second cutout; and

a third cutout curved to define both a long edge and a short edge of one of the subareas.